

A New Pulsar Timer

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The times-of-arrival of pulses of radiation from pulsating radio sources (pulsars) have been measured at the Venus Deep Space Station (DSS) by Downs and Reichley (Ref. 1). This article describes a programmable high-speed timing source, designed to control the data sampling. A possible use of the timer, as part of a DSN navigation system, is to determine a spacecraft's position in inertial space. It is easily controllable by computer and is intended to be part of a demonstration of remote experiment operation in which the Sigma 5 at JPL will configure pulsar experiments at DSS 13.

I. Introduction

This article describes a new timer that operates under program control of the XDS 930 computer, providing entirely variable major and minor cycle pulse rates, with automatic start, delay, and stop features. Incorporating a fast analog-to-digital converter (ADC), with a maximum sampling rate of 250 kHz, and having a selectable sampling interval within each period, the duty cycle of the sampling scheme can now be more closely matched to that of the pulsar. Data resolution is thus improved by over a factor of 10, to 4 μ s per sample. Signals are also available from the timer to control the operation of the noise-adding radiometer (Ref. 2), which functions in complement with pulsar sampling. It is intended to demon-

strate this timer in an experiment in which DSS 13 is remotely configured from the Sigma 5 at JPL.

A suggested novel use of the timer is as part of a DSN radio navigation system. Comparison of times-of-arrival of three pulsars (approximately orthogonal to the craft) measured on board and on Earth gives an accurate fix of the spacecraft's position relative to Earth when simultaneous ranging is carried out.

II. System Description

The times-of-arrival of pulses of radiation from pulsating radio sources are measured relative to a 1-s pulse derived from a cesium standard operating at 1 MHz and

accurate to 1 part in 10^{12} . The 1-MHz signal from the cesium standard also drives a frequency synthesizer. In the existing system, an operator presets the frequency synthesizer for $f_p \times 10^6$ Hz, where f_p is the apparent pulsar frequency, and then arms a start gate, which allows the cesium clock to trigger the sampling of data at a predetermined time. The frequency of the synthesizer output is divided to produce signals controlling the data sampling.

As shown in Fig. 1, the synthesizer signal is divided by $D1$, giving the major cycle signal, f_{major} , at a frequency $(f_p \times 10^6)/D1$ Hz, and by $D2$, giving the basic minor cycle timing signal. The minor cycle signal externally drives the ADC, and hence, $(f_p \times 10^6)/D2$ samples are obtained per pulsar period. These samples are uniformly distributed over a given period, and since the actual pulsar width lies well within the period (typically, pulsar duty cycles are about 5%), the sampling is not optimized over the region of interest. Furthermore, the major cycle divisor is fixed ($D1 = 10^6$), and there are only four available values for $D2$, namely, 200, 100, 50, and 25, with a maximum ADC sampling rate of 20 kHz.

The new timer similarly divides down the synthesizer signal to create f_{major} and f_{minor} . The interface to the XDS computer allows for variable dividers and complete control over pulsar data sampling and subsequent processing in the machine.

A. Software

A flow chart of the pulsar timer program *PUT*, written in SYMBOL assembly language for the XDS 930 computer, is shown in Fig. 2. Given the following integer parameters, entered with individual requests on the typewriter, the program allows for complete control of all data flow into the machine, subsequent integration, processing, and output of data. Automatic start, delay, or stop during any operation is obtained without loss of time sync with the pulsar data.

TS = Start time (GMT) (entered as a 6-digit integer)

X = major cycle divisor

Y = minor cycle divisor

Δ = sampling delay (in number of minor cycle pulses)

ΔL = sampling length (in number of minor cycle pulses)

N = pulse integration number (in number of major cycle pulses)

f_s = synthesizer frequency (Hz)

From the above,

$$f_{\text{major}} = \frac{f_s}{X}, \quad f_{\text{minor}} = \frac{f_s}{Y}$$

The limiting values for the parameters are listed below:

$$00:00:00 \leq TS \leq 23:59:59$$

$$1 \leq X < 10^8$$

$$1 \leq Y < 2^{20} \quad Y < \frac{X}{Y} < 2^{20}$$

$$0 \leq \Delta < 2^{20}$$

$$0 \leq \Delta L < 2^{20} \quad \Delta < \Delta + \Delta L < 2^{20}$$

$$0 < N < 2^{12}$$

Thus, for each of N major cycles, after a sampling delay of Δ minor cycle pulses, ΔL samples of pulsar data are taken at the minor cycle rate and stored in core. At this point, data flow into core is halted, and the data in core are integrated and loaded onto magnetic tape, while the hardware maintains time sync by monitoring major cycle pulses. After all further processing (plotting, etc.) is completed and the time required for the processing recorded on magnetic tape, data flow into core is resumed with the original divider parameters intact.

The breakpoints on the console allow for the following interruptions:

BPT 2: SET for DELAY. The program allows data flow into core for the current major cycle. At the end of this cycle, the program stops data flow. Time sync is maintained by the timer until either BPT 2 is RESET, or BPT 4 is SET. In the former instance, data flow into core is resumed, the delay time is written on tape, and the pulse integration number counter is reset to zero. In the latter case, time sync is abandoned, and the program enters the HALT state.

BPT 3: SET for accumulation. The program accumulates data samples in core for as many periods as BPT 3 is SET. With BPT 3 RESET, core is cleared before each period of N major cycles of data.

BPT 4: SET for immediate HALT. The program stops data flow into core and tests for BPT 4 to be RESET, indicating a RESTART. No time sync is maintained, since this is considered an emergency stop. At RESTART, all breakpoints should be in the RESET position.

B. Hardware

A block sketch of the pulsar timer hardware appears in Fig. 3. The program reads the TS clock (which is synced with the cesium standard), and upon reaching the pre-programmed start time (TS) minus 1 s, arms a start gate. Sampling of data commences on the next 1-s pulse from the TS clock. The first two programmable dividers with 20-bit binary divisors reduce the input signal from a frequency of $f_p \times 10^6$ Hz to create the minor cycle signal at a frequency $(f_p \times 10^6)/Y$ Hz and the major cycle signal at a frequency $(f_p \times 10^6)/X$ Hz.

High-speed switching of data from the Δ and $\Delta + \Delta L$ registers into the third programmable divider via the multiplexer allows for this divider to perform the dual function of deleting Δ pulses and passing ΔL pulses. During each major cycle, a count of Δ minor cycle pulses enables the output gate G . This enabling signal also switches the $\Delta + \Delta L$ divisor into the divider in midstream. When the count reaches $\Delta + \Delta L$, gate G is disabled and the output is terminated until the next major cycle pulse.

The fourth divider, which is limited to a 12-bit binary divisor $[N]$, provides a $2\text{-}\mu\text{s}$ interrupt to the computer when the count equals the pulse integration number. In a delay mode, the divide function is inhibited via the

delay gate, gate G is disabled, and the divider merely counts major cycle pulses, thus maintaining sync with the clock. Upon termination of the delay, the program accesses the current number in the counter via a read gate, resets the counter to zero, and reactivates the divide function. The major cycle signal is also sent to the program via an interrupt line to provide appropriate timing for the control of the N divider, as described.

III. System Performance

Preliminary checkout of the timer was performed at JPL and at the Venus Deep Space Station, utilizing a known pulse source as a pseudo-pulsar. Various sampling rates (to a maximum 20 kHz, limited by the ADC) and duty cycles were tested. The program and timer performed to specifications. With the divisors set to their upper-limit values, the timer has a maximum operating speed of about 14 MHz. The basic limitation is the speed of the comparators used in the divider design. With the divisors set to their lower-limit values, 20-MHz operating speed is achieved, which is the upper speed limit on the integrated circuits used.

Delivery of a high-speed ADC is expected shortly, at which time results of high-speed-sampled pulsars will be published.

References

1. Reichley, P. E., Downs, G. S., and Morris, G. A., "Time of Arrival Observations of Eleven Pulsars," *Astrophys. J.*, Vol. 159, Jan. 1970.
2. Batelaan, P. D., Goldstein, R. M., and Stelzreid, C. T., "A Noise-Adding Radiometer for Use in the DSN," in *The Deep Space Network*, Space Programs Summary 37-65, Vol. II, pp. 66-69, Jet Propulsion Laboratory, Pasadena, Calif., Sept. 30, 1970.

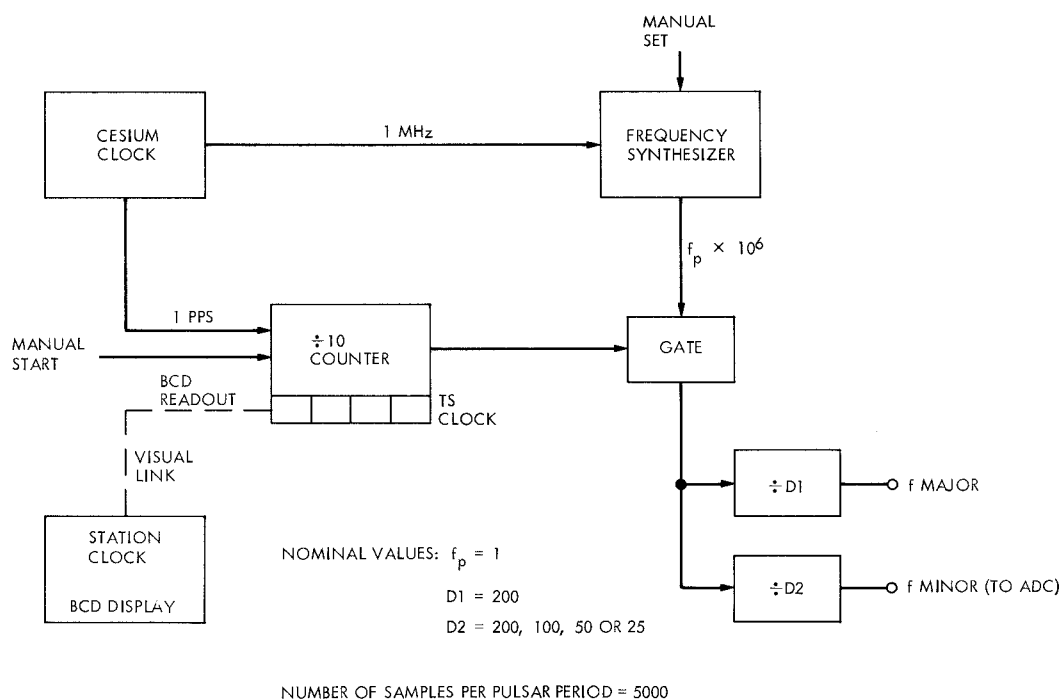


Fig. 1. Old timer functions

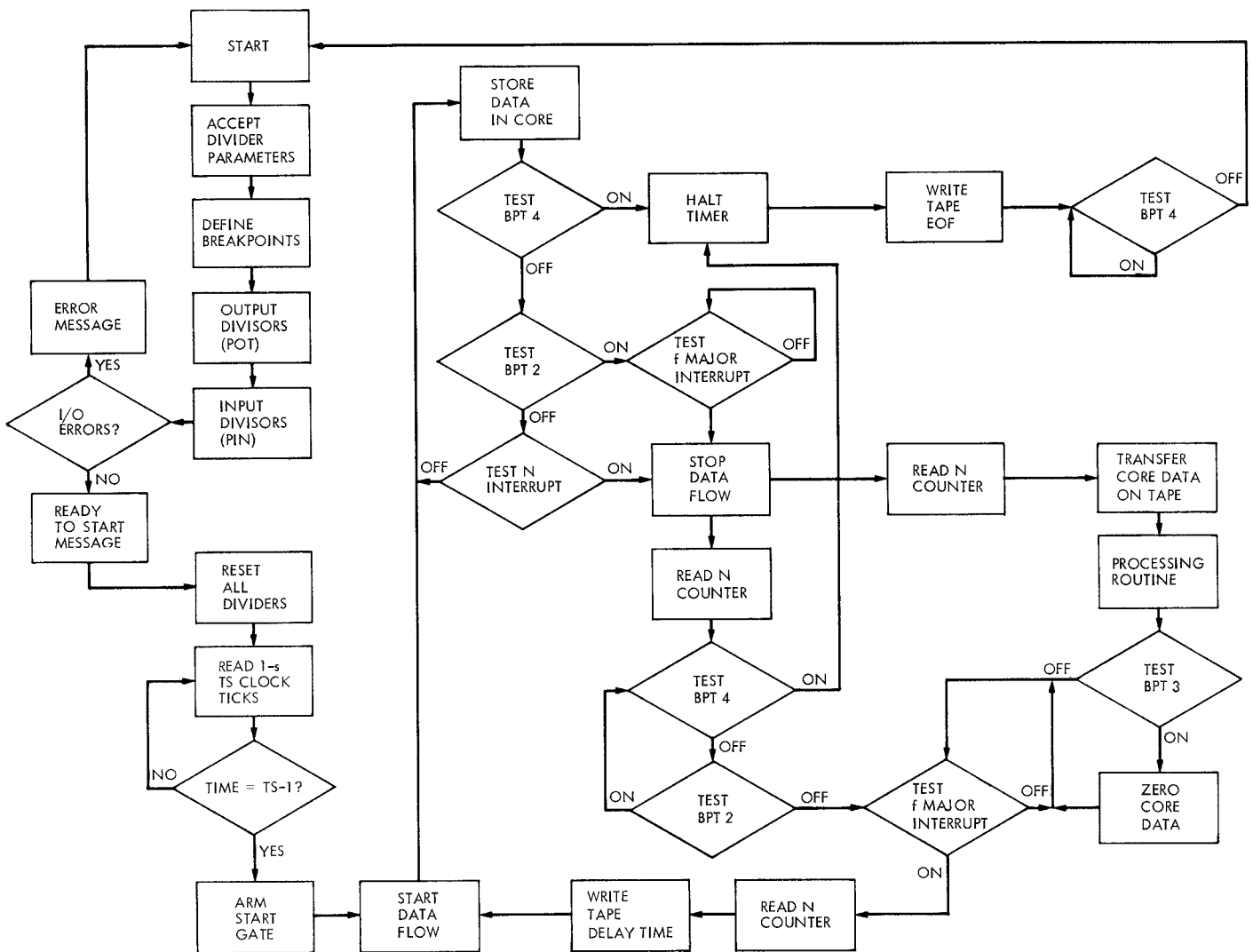


Fig. 2. Pulsar timer program *PUT*

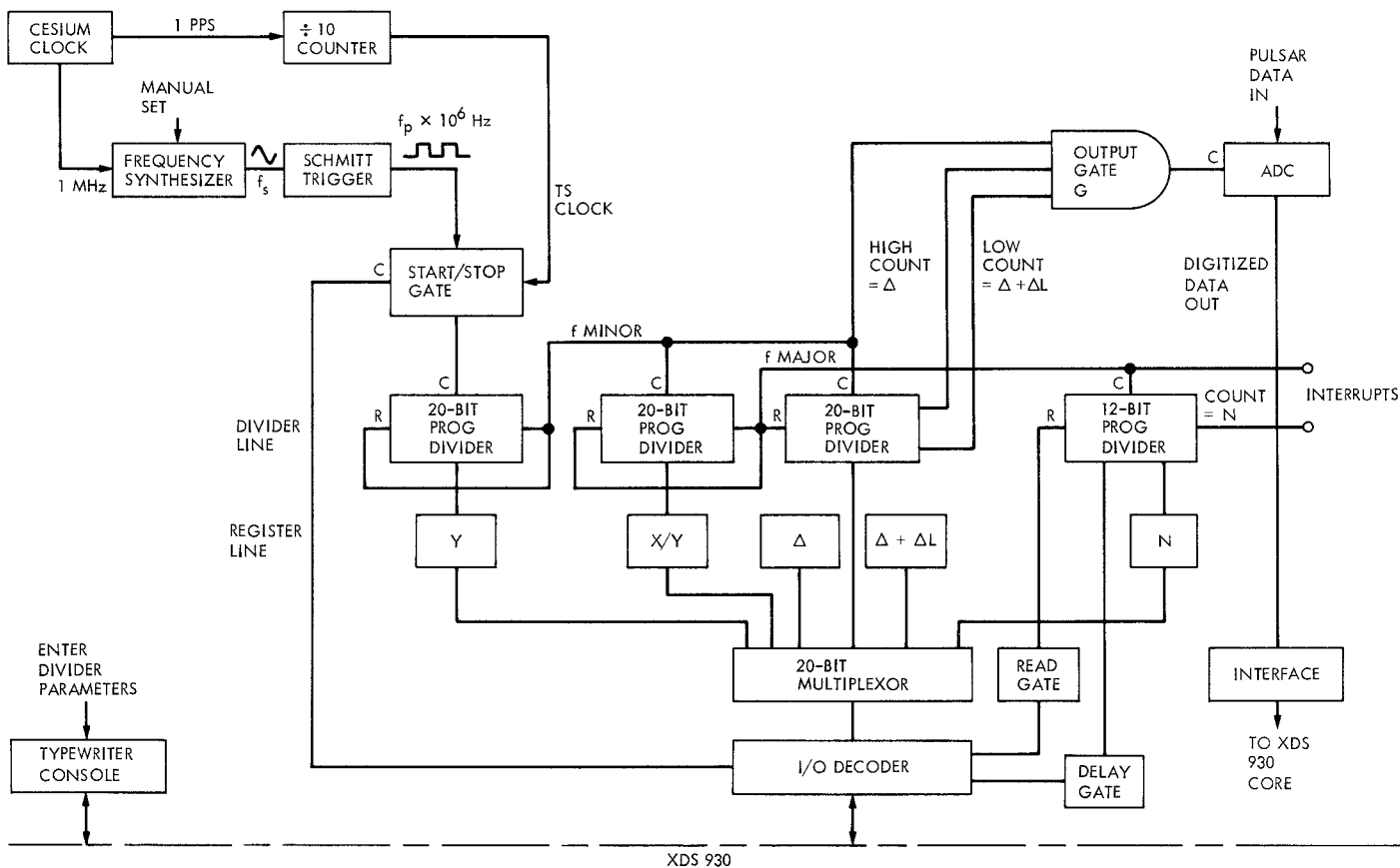


Fig. 3. Pulsar timer hardware